REMARKS

Claims 1, 2, 4-10, 15, and 17-19 are in the application, with Claims 3, 11-14, and 16 having been cancelled and Claims 1, 4, 5, 8, 10, 15, 17, and 18 having been amended. Claims 1, 8 and 15 are the independent claims herein. No new matter has been added. Reconsideration and further examination are respectfully requested.

Claims 1-9 stand rejected under 35 U.S.C. §102(b) as allegedly being anticipated by U.S. Patent No. 6,489,676 ("Taniguchi"); claim 10 is rejected as being unpatentable under 35 U.S.C. §103(a) over Taniguchi in view of U.S. Patent No. 5,422,435 ("Takiar"); and Claims 15-19 are rejected as being unpatentable over Taniguchi in view of U.S. Publication No. 2002/0196650 ("Chang"). Reconsideration and withdrawal of the rejections are respectfully requested.

Claims 1 and 15

Claim 1 concerns an apparatus including an integrated circuit die, an integrated circuit package coupled to the integrated circuit die, mold compound in contact with the integrated circuit die and the integrated circuit package, and an interconnect in contact with the integrated circuit package. The apparatus also includes a second integrated circuit package and a second interconnect in contact with the second integrated circuit package. A first portion of the interconnect is in contact with the mold compound, and a second portion of the interconnect is not in contact with the mold compound. The mold compound defines an opening, and the second portion of the interconnect is recessed beneath the opening. Additionally, a third portion of the interconnect is in contact with the integrated circuit package, and the second interconnect is in contact with the interconnect within the opening.

As previously described, some embodiments of the foregoing features may provide packages of less vertical height than previously available.

The art of record is not seen to disclose or suggest the features of Claim 1. In particular, the cited art is not seen to disclose or suggest mold compound defining an opening, in which a second portion of an interconnect in contact with the integrated circuit package is not in contact with the mold compound and is recessed beneath the opening, and in which a second

interconnect in contact with a second integrated circuit package is in contact with the interconnect within the opening.

Taniguchi describes semiconductor devices that may be vertically stacked to provide a multi-die system. FIGS. 8 and 9 of Taniguchi show semiconductor devices 20b and 20c, each including copper posts 18a and 18b. As described at col. 7, lines 30-34, a height of post 18a is less than a height of sealing resin 8, resulting in post hole 30. Post 18b, however, is then formed in post hole 30 (col. 7, lines 38-39) such that an end of post 18b is "exposed on the outer surface of sealing resin 8" (col. 7, lines 58-59). Accordingly, when several instances of semiconductor devices 20b or 20c are stacked together, solder balls 6 of an upper semiconductor device contact the ends of corresponding posts 18b of a lower device. As shown in FIGS. 12 and 13, this contact occurs at the upper surface of sealing resin 8. Therefore, Taniguchi does not describe an opening in which an interconnect that is in contact with a first integrated circuit package contacts a second interconnect that is in contact with a second integrated circuit package.

Amended Claim 1 and its associated dependent claims are therefore believed to be allowable.

Amended Claim 15 also concerns suggest mold compound defining an opening, in which a second portion of an interconnect in contact with the integrated circuit package is not in contact with the mold compound and is recessed beneath the opening, and in which a second interconnect in contact with a second integrated circuit package is in contact with the interconnect within the opening. Claim 15 was rejected over Taniguchi in view of Chang. As Chang is not seen to remedy the above-described deficiencies in Taniguchi, Claim 15 and its dependent claims are also believed to be allowable.

Claim 8

Claim 8 concerns an apparatus that includes an integrated circuit package substrate. A plurality of integrated circuit die is coupled to the integrated circuit package substrate. A mold compound is in contact with the plurality of integrated circuit die and the integrated circuit package substrate. An interconnect is in contact with the integrated circuit package substrate and electrically coupled to one of the plurality of integrated circuit die. The apparatus also includes a

second integrated circuit package, and a second interconnect in contact with the second integrated circuit package. A first portion of the interconnect is in contact with the mold compound, a second portion of the interconnect is not in contact with the mold compound, and the mold compound defines an opening. The second portion of the interconnect is recessed beneath the opening, a third portion of the interconnect is in contact with the integrated circuit package substrate, and the second interconnect is in contact with the interconnect within the opening.

As described above, Taniguchi is only seen to describe a system in which an interconnect (i.e., solder ball 6) coupled to a second integrated circuit package contacts an interconnect (i.e., post 18a or post 18b) coupled to a first integrated circuit package at an upper surface of sealing resin 8. Accordingly, Taniguchi cannot be seen to disclose or to suggest mold compound defining an opening, a second portion of an interconnect in contact with an integrated circuit package that is not in contact with the mold compound and is recessed beneath the opening, and a second interconnect in contact with a second integrated circuit package that is in contact with the interconnect within the opening. Claim 8 and all claims depending therefrom are believed to be in condition for allowance.

CONCLUSION

The outstanding Office Action presents a number of characterizations regarding each of the applied references, some of which are not directly addressed herein because they are not related to the rejections of the independent claims. Applicants do not necessarily agree with the characterizations and reserve the right to further discuss those characterizations.

For at least the reasons given above, it is submitted that the entire application is in condition for allowance and such action is respectfully requested at the Examiner's earliest convenience. Alternatively, if there remains any question regarding the present application or any of the cited references, or if the Examiner has any further suggestions for expediting allowance of the present application, the Examiner is cordially requested to contact the undersigned via telephone at (203) 972-0049.

Respectfully submitted,

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